II. Remarks

Reconsideration and re-examination of this application in view of the above amendments and the following remarks is herein respectfully requested.

After entering this amendment, claims 1-7 and 9-17 remain pending.

Claim Rejections - 35 U.S.C. § 102(b)and 35 U.S.C. §103(a

Claims 1, 4-6, 9-12, and 14-17 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,301,687, to Jain, et al. ("Jain"). Claims 2, 3, and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Jain in view of U.S. Patent No. 6,993,730 to Higgins, et al. ("Higgins"). Applicants respectfully traverse these rejections.

The Office Action states that Jain teaches "determining for specific circuit structures described by the reference description of the digital circuit, for which different implementation alternatives are known, in each case (that) an implementation alternative that has the greatest degree of structural equivalence with the digital circuit to be verified, is determined ... ."

First, the Office Action points out that the "different implementations of the same design" as disclosed in column 1, line 51 to 54 of Jain would be known and that one implementation alternative which has the greatest degree of structural equivalence would correspond to checking equivalence by verifying the different implementations as disclosed in column 1 line 54 to 55 of Jain. The Office Action further points out that limitations from the specification do not read into the claims

and that therefore an implementation alternative is not understood as one alternative of a plurality of possible alternative.

In an effort to better clarify the claimed invention, the applicant has amended the independent claims to clearly recite that a first implementation alternative out of a plurality of different pre-defined implementation alternatives is determined in order overcome this objections and to clearly state that one specific alternative out of a plurality of implementation alternatives is determined and later on selected for replacement the reference description.

Jain discloses the use of a plurality of different implementations on after the other, wherein a new implementation is verified against the current specification and, in case the verification hold true, the implementation replaces the original specification. Jain et al discloses a verification process, the outcome of which is either true or wrong. In case the outcome of verification is true, the specification is replaced, in case the outcome is wrong, no replacement may be made. However, Jain discloses the use of only one implementation at a time that is compared to the current description. In contrast, the present invention claims a determination process to determine and choose from a plurality of different alternatives the one alternative that fits best, i.e. that has the greatest degree of structural equivalence with the digital circuit to be verified. Thus the outcome of the verification step is: implementation alternative X fits best. Such a determination process is not disclosed in Jain.

Next, the Office Action points out that the specification states that implementation alternatives possibly have only a few internal equivalents and that

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Jain would analogously disclose internal equivalences of two networks. The applicant respectfully disagrees. Jain relates to the formation of a composite network from two given networks N1 and N2 by joining corresponding primary inputs and verifying equivalence of same notes as referred to in column 6, lines 25 to 45 of Jain. However, this does not relate to the different implementation alternatives referred to in column 1 lines 47 to 60 of Jain. The networks therefore do not relate to the implementation alternatives of the present invention.

The independent claims have also been amended further amended to now recite that the first implementation alternative is determined from one of a plurality of pre-defined implementation alternatives. Predefined implementation alternatives are disclosed one page 7, lines 7 to 8 of the originally filed description. This clearly points out that the implementation alternatives are pre-defined and known prior to the method of the invention. These pre-defined implementation alternatives are different architectural structures that fulfill the same function in the circuit but might have only a few internal structural equivalences. In contrast, Jain et al teaches the use of different implementations that are verified once they have been found in order to replace the current specification. Jain does not disclose any pre-defined implementation alternative.

The Office Action further points out that plurality of possible alternatives to implement a specific function would be in fact the same circuit function being implemented in each alternative, which Jain et al would teach as different implementations of the same design. The applicant agrees that Jain et al describes different implementations of the same design that are compared (verified) one by

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one to check their equivalence. However, this different implementation cannot be used alternatively, but only one at a time as they are replaced subsequently (column 1, line 54 to 61 of Jain). In contrast, the implementation alternatives according to the present invention are set of a plurality of different pre-defined implementation alternatives that can be determined and consequently selected as alternatives. The applicant has amended the claims to clearly recite that one implementation alternative out of a plurality of possible implementation alternatives is determined and then this one is chosen and replaced in the description of the circuit. This is not disclosed or suggested in Jain et al.

Furthermore the Office Action points out that an implementation with the greatest degree of structural equivalence would be determined as a result of columns 1, lines 45 to 60 of Jain. The applicant agrees that Jain discloses that a first implementation of a circuit is compared to an original specification and, if that first implementation is equivalent then the first implementation replaces the original specification, and then the new original specification is compared for equivalence to the second implementation and so on.

The Office Action further points out that this replacement of a specification by an implementation would continue until the original specification is replaced with an implementation that is of the highest degree of structural equivalence. The applicant respectfully disagrees. Jain teaches the replacement of a specification by an implementation that is verified against this original specification. This means, that the implementation does correspond to the original specification and therefore can replace the specification if verification was successful. As stated above, a verification

process can only give a result "verified" or "not verified" which allows for replacement or not. Thus, Jain does not teach any degree of equivalence and in particular no degree of structural equivalence. Claim 1 has been amended to clearly recite that, out of the different parallel implementation alternatives, the (first) implementation alternative is determined and consequently selected that has, compared to the others, the highest degree of structural equivalence. Jain et al does not disclose any selection or determination of a specific alternative having the highest degree compared to the others. In contrast, the different implementations of the same design according to Jain all have the same functionality that is verified against an original specification. Therefore Jain does not disclose the subject matter of present claim 1.

Next, the Office Action points out, that he interprets the term "replacing in the reference of the digital circuit the description of the individual circuit structures by the implementation alternatives determined for the respective circuit structure" as replacing the entirety of the description by individual structures one at time until the entire description is replaced. As suggested by the Office Action the claim language has been amended to clarify that the at least one specific structure is a portion of the digital circuit. Thus, the amended claim clearly states that it is not the entire digital circuit that is replaced. Also, therefore the present invention is novel over Jain.

Besides the above-mentioned differences, the present invention has a different concept compared to the method used in Jain. Jain uses a simulation wherein different descriptions, referred to as implementations in Jain are verified with respect to each other and are subsequently replaced by each other in order to obtain

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a modified description of the digital circuit. Furthermore Jain describes the comparison and the composition of different descriptions. This method is used in many equivalence tests and might also be applied during the step of executing the equivalence test of present claim 1.

In contrast, the present application describes a method that can be used as a preparation for the equivalence test and thus prior for the method of Jain. According to the present invention, simulation can be considerably simplified for a specific circuit structure if a plurality of specific implementation alternatives is known. For example, if a specific circuit structure corresponds to a multiplier, there are a limited number of actual implementations (how this multiplier can be realized on the chip layout) that is known for a chip design. These implementation alternatives are pre-defined as they are all known at the same time prior to the verification process. The method according to the invention now determines and chooses out of the plurality of pre-defined implementation alternatives the one having the highest structural equivalence with the digital circuit to be verified. This is the alternative that is most likely being implemented in the actual chip. The present invention suggests replacing the specific circuit structure by the determined implementation alternative in order to consider and simplify the verification process (as mentioned in step (c) of present claim 1).

The applicant notes, that the comparison of the digital circuit with the reference description modified according to step (a) and (b) of present claim 1 may be executed (as an example) by the method according to Jain. However, many alternative methods are known in the art.

Jain does not disclose a simulation to find out the most suitable implementation alternative from a plurality of implementation alternatives prior to an equivalence test that is carried out with the selected one of the implementation alternatives. The present invention is therefore novel in view of Jain.

As discussed above, the present invention as claimed in amended claim 1 differs in several substantial features from Jain. Consequently, the present invention is neither anticipated nor suggested by Jain et al and thus patentable over Jain et al. As claim 1 is patentable dependent claims 2 to 13 are patentable as well. The corresponding independent claims 14 to 17 have been amended according to the amendments of claim 1 and are therefore patentable as well.

Conclusion

In view of the above amendments and remarks, it is respectfully submitted that the present form of the claims are patentably distinguishable over the art of record and that this application is now in condition for allowance. Such action is requested.

Respectfully submitted,

January 15, 2009
Date

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Attachments: None

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